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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,784	11/13/2003	Chris B. Freeman	5038-327	8754

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EXAMINER	
DINH, NGOC V	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,784	FREEMAN ET AL.	
	Examiner	Art Unit	
	NGOC V. DINH	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-9,11-14,16-25 and 27-31* is/are rejected.

7)☒ Claim(s) *3-4,10,15 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is a response to the U.S. application Serial No. 10/713784 filed on 11/13/2003. Claims 1-31 are presented for examination.

INFORMATION DISCLOSURE STATEMENT

2. The Applicant's submission of the IDS filed 03/20/2004 have been considered. As required by M.P.E.P. 609 C(2), a copy of the PTOL-1449 is attached to the instant office action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-2, 5, 9, 11, 16-19, 21-25, 27, 29-31 are rejected under 35 U.S.C.102 (e) as being anticipated by Perego et al PN 7,062,597.

As per claim 1, Perego teaches: a memory module buffer [buffer device, 350, fig. 3A-3B; fig. 5; col. 5, lines 1-5] comprising:

a host-side memory channel port [At least one point-to-point link connects at least one memory subsystem to the master, (e.g., a processor or controller), col. 5, lines 17-25; 510, fig. 5] and a memory device channel port [port 370 connected to plurality memory device, fig. 3B; col. 8, lines 14-20];

a command decoder to decode commands received at the host-side memory channel port [540, request& address logic connected to point-to-point link (510), fig. 5, wherein point-to-point link is a host-side memory channel port receiving request from host CPU as mentioned above]

the commands including at least one implicit command type [buffer device 350 transceives and provides isolation between signals interfacing to controller 310, col. 6, lines 27-29; wherein implicit command is the command that processor generates to the controller] and

a memory device access controller [memory controller, fig. 1, fig. 2B; 310, fig. 3A-3B; Memory systems 300 and 305 include a controller 310, a plurality of point-to-point links 320a-320n, col. 5, lines 49-55] to respond to a command having an implicit command type [host side processor issues request command through memory controller 310, col. 5, lines 17-25; Controller 310 receives the signals corresponding to the data at corresponding port 378a-378n, col. 6, lines 39-40] by generating at least one explicit memory access command [buffer device 510, fig 5 to the memory device channel port [buffer device 350 transceives and provides isolation between signals interfacing to the plurality of memory devices 360, col. 6, lines 27-30; wherein explicit command is the command that buffer device generates to plurality of memory devices, col. 6, lines 27-45].

As per claims 2 and 25, Perego teaches the at least one implicit command type includes at least one implicit write command [write operation, col. 9, lines 1-3; control lines (RQ) transport control (e.g., read, write, precharge . . .) information and address (e.g., row and column), col. 8, lines 39-41] with a command format that specifies a first region of memory [information and address (e.g., row and column), col. 8, lines 40-45] to be written to, the buffer further comprising a write data generator [write buffer, fig. 5; col. 10, line 67 to col. 11, line 5] to form implicit write data in accordance with the implicit write command. The further claimed limitation " and includes less explicit write data than would be needed to fill the region of memory" appears to be inherent in Perego's system. This is because in order to avoid buffer overflow, the size of write data (bytes) should be less than the size of allocated memory associated with this write data.

As per claim 5, Perego teaches the at least one implicit write command includes a command comprising a data value [see claim 2 above]. The further claimed limitation " and wherein the write data generator forms implicit write data by repeating the data value for multiple addresses throughout the first region of memory" appears to be inherent in Perego's

system. This is because the computer system today utilizes a read/write burst mode, wherein burst write can make data transfer within a single signal from several tracks/banks ("forms implicit write data by repeating the data value for multiple addresses", claimed invention) simultaneously. By buffering multiple writes ("implicit data by repeating the data value", claimed invention) and then writing all buffered write data in a single burst, the write turnaround penalty of the memory module's data bus is substantially minimized.

As per claims 11 and 23, Perego teaches the write data generator comprises an error correction code generator capable of generating an error correction code as part of an implicit write data word [ECC, col. 9, lines 38-42].

As per claim 16, Perego teaches a method of writing data [write operation, col. 9, lines 1-3, fig. 3A] to memory on a buffered memory [memory subsystems 330a-330n are buffered modules, fig. 3B, col. 6, lines 40-45] module the method comprising:

receiving, at a buffer on the module, a command specifying an implicit [signal interface to controller 310 col. 6, lines 27-30] write to the memory [write operation, write data, col. 11, lines 1-5];

in response to the implicit command, forming at least one first data word/first write address combination for an explicit [signals interfacing to the plurality of memory devices 360, col. 6, lines 29-30] write [write operation, col. 9, lines 1-3] to the memory; and transmitting the data word and write address to the memory as part of a first explicit write command [One of memory subsystem ports 378a-378n includes I/Os, for sending and receiving data, addressing and control information over one of point-to-point links 320a-320n, col. 5, lines 62-65; One of memory subsystem ports 378a-378n includes I/Os, for sending and receiving data, addressing and control information over one of point-to-point links 320a-320n; write buffer 550 may improve interfacing efficiency by utilizing available data transport windows over point-to-point link 320 to receive write data and optional address/mask information, col. 10, line 67 to col. 11, line 5].

As per claims 17-18, reading a stored data word from the memory in response to the implicit command; and forming the at least one data word using the stored data word [col. 6, lines 27-35] are repeated for multiple memory locations in response to the implicit command [col. 6, lines 30-35].

As per claim 19, forming at least one data word/write address combination for an explicit write to the memory [col. 5, lines 62-65]. The further claimed limitation "comprises repeating a data value specified by the implicit command for multiple write addresses" appear to be inherent in Perego's system as explained in claim 5.

As per claim 21, forming at least one data word/write address combination comprises forming a data word that at least partially depends on the write address [row/column addressing and read/write commands, col. 1, lines 39-41; data word/write address combination depends at least row or column of write address].

As per claims 9 and 22, the further claimed limitation "the command specifies multiple non-contiguous sub-regions of memory, the method further comprising transmitting a second data word and second write address to the memory as part of a second explicit write command, the second write address non-contiguous with the first write address" appears to be inherent in Perego's system. This is because a write operation comprises write command and its associated data word and address, and the write command will transmit its associated data word and address to its destination. When commands (e.g., write command) are successfully executed. The successive commands are addressed to several areas of the memory contiguously and non-contiguously depending on the available of memory (either contiguous or non-contiguous address) which is allocated by the memory controller or OS at the time commands are executed. The OS may control all allocation of commands (read and write) access to at least a predetermined physical portion of the memory either contiguous or non-contiguous which is available for allocation for use by instances of application programs or other processes.

As per claims 24 and 30, Perego teaches the claimed limitations as mentioned in claim 1 and further teaches: a computing device comprising:

a processor [col. 10, line 64];

a buffered memory module [memory subsystems 330a-330n are buffered modules, fig. 3A-B, col. 6, lines 40-41] comprising: a plurality of memory devices [fig. 3B] and a buffer [360, fig. 3A] connected to the memory device [350, fig. 3A];

a first point-to-point memory channel coupling the processor to the buffered memory module [510, fig. 5].

As per claim 27, Perego teaches the claimed method of steps in claim 16. Therefore, Perego teaches a computer readable-media of claim 27 to carry out the method of steps.

As per claim 28, the claimed limitation "the implicit memory command specifies a start address, read length, skip length, and number of sub regions to read, the method further comprising processing a block of read data returned by the buffered memory module with knowledge of the read and skip length" appears to be inherent in Perego's system. This is because in the modern computer system, sequential transfer modes such as a burst mode, are often used to improve system throughput in data intensive applications. In this manner, the processor performs burst read operations in both a sequential and a non-sequential. The burst mode utilizes a dynamic burst length calculating method to calculate the burst length (word deep, start/end address) of read command. The counter in the address generator of the burst mode keeps track of the current and next address (number of sub regions to read) where the read operation is currently executed by using a jump command (skip length) to ensure the length of the data byte does not exceed the size of the allocated memory when burst read operation is in non-sequential manner.

As per claim 29, Perego teaches the implicit memory command specifies a write command and indicates how the buffered memory module is to construct write data and/or write addresses for multiple write cycles [col. 10, line 58 to col. 11, line 5].

As per claim 31, Perego teaches the buffer on the first buffered memory module further [fig 8B] comprises a downstream memory channel port [960c, fig 8B], the computing device further comprising:

a second buffered memory module [950b, fig. 8B] having a host-side memory channel port; and

a second point-to-point memory channel [960b, fig. 8B] connecting the first buffered memory module downstream memory channel port to the second buffered memory module host-side memory channel port; the computing device having the capability to issue an implicit command to the first memory module and issue another command through the first memory module to the second memory module while the first memory module is executing explicit commands in response to the implicit command [col. 12, line 48 to col. 13, line 10].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 13 is rejected under 35 U.S.C 103(a) as being unpatentable over Perego.

As per claim 13, Perego dose not explicitly teach the memory module buffer of claim 1, further comprising a pause function activated by the command decoder when a second command requiring access to the memory device channel port is received during activity related to a first command of an implicit command type, the memory device access controller responding to the pause function by pausing execution of the first command while the second command executes.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further include an Interrupt Function (Pause Function) into Perego's system in order to interrupt the execution of one command (low priority) and start executing

other command (higher priority). Doing so would prevent low priority device from being starved from access to the resource.

5. Claim 14 is rejected under 35 U.S.C 103(a) as being unpatentable over Perego, and in view of Anderson PN 6,523,098.

As per claim 14, Perego dose not explicitly teach the memory module buffer further comprising a completion register that the memory module buffer sets to indicate the status of a pending command with an implicit command type, wherein the value stored in the completion register is accessible from the host-side memory channel port.

Anderson teaches a register for indicating the status of a pending command [status of pending requests for a high priority operation, col. 1, lines 55-60; col. 1, lines 35-50] with an implicit command type [the processor 202, fig. 2 generates command through memory controller 210, fig. 2, wherein memory controller includes a pending high priority operation detector, 104, fig. 3], wherein the value stored in the completion register is accessible from the host-side memory channel port [col. 3, lines 55-65].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include the teaching of Anderson, as mentioned above into Perego's system so that pending command with high-priority will be serviced before any other pending command.

6. Claims 6-8 and 20 are rejected under 35 U.S.C 103(a) as being unpatentable over Perego, and in view of Langendorf PN 6,820,087.

As per claims 6-8 and 20, Perego dose not explicitly teach a pattern register coupled to the write data generator to store the predefined pattern; at least one implicit write command includes a command indicating that a predefined pattern is to be written to the first region of memory, and wherein the write data generator forms implicit write data by repetitively

generating the predefined pattern; the data value specified by the implicit command is determined by reading a value from a pattern register.

Langendorf teaches a pattern register [745, fig. 7] coupled to a write generator [initial/copy device 740, fig. 7] to store predefined pattern [write transaction to load the predetermined pattern into the pattern register, col. 8. claim 11]; at least one implicit write command includes a command indicating that a predefined pattern is to be written to the first region of memory, and wherein the write data generator forms implicit write data by repetitively generating the predefined pattern; the data value specified by the implicit command is determined by reading a value from a pattern register [The memory access engine writes a predetermined pattern to a data structure located in a memory device. The data structure is defined by the start address, col. 2, lines 59-65; col. 5, lines 15-20; col. 6, lines 1-15]

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include the teaching of Langendorf, as mentioned above, into Perego's system in order to minimize the intervention of the processor, thus free the processor for performing other task [col. 5, line 55-60].

7. Claim 12 is rejected under 35 U.S.C 103(a) as being unpatentable over Perego, and in view of Nataraj et al US PUB 2005/0262295.

As per claim 12, Perego does not teach the memory device channel port having a data width, the buffer further comprising a data mask generator to mask a portion of the data width during writes responsive to an implicit command type when an implicit command specifies a partial-width write command.

Nataraj teaches a buffer comprising a data mask [CAM with mask, 1500 fig. 15; CAM array 1501 can be configured into n different ZY/n width, col. 13 [0169]; The CAM system may also include one or more global mask registers, The instructions may include instructions to program the word width and other operating parameters of the CAM device 1500, instructions to write data or mask word, col. 14, [0176].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include the teaching of Nataraj in to Perego's system so that only significant data bits being search during write operation (least significant bits being ignored) thus latency write access is reduced.

Allowable Subject Matter

8. Claims 3-4, 10, 15, 26 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. **Any response to this action should be mailed to:**

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PMR) system. Status information for published Applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http//pak-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (571) 272-4191. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon, can be reached on (571) 272-4204.

NGOC DINH
Patent Examiner
ART UNIT 2189
August 31, 2006

REGINALD BRAGDON
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